IOSR Journal of Engineering
June. 2012, Vol. 2(6) pp: 1301-1307

A Carrier Overlapping PWM Technique for Seven Level Asymmetrical Multilevel Inverter with various References

Johnson Uthayakumar R.[1], **Natarajan S.P.**[2], **Bensraj R.**[3]
[1]*Research Scholar, Department of Electronics and Instrumentation Engineering, Annamalai University.*
[2]*Professor and Head, Department of Electronics and Instrumentation Engineering, Annamalai University*
[3]*Assistant Professor, Department of Electrical and Electronics Engineering, Annamalai University*

ABSTRACT
This paper presents the use of Control Freedom Degree (CFD) combination to evaluate the performance of single phase seven level Asymmetrical MultiLevel Inverter (AMLI) fed with resistive load. The effectiveness of the Pulse Width Modulation (PWM) strategies developed using CFD are demonstrated by simulation. The results are compared for sine, trapezoidal and Trapezoidal Amalgamated Reference (TAR) references in the Carrier Over Lapping (COPWM) strategy. By the different pattern of overlapping it is classified as carrier overlapping, Type-A, Type-B and Type-C. The Total Harmonic Distortion (THD) the Root Mean Square (RMS) value and Form Factor (FF) of output voltage are analyzed for modulation indices 0.7-1. The simulation results indicate that the use of CFD combination is an important clue to realize high performance multilevel inverters.

Keywords *- COPWM-A,COPWM-B,COPWM-C,THD,RMS*

I. INTRODUCTION
Multi Level Inverters (MLI) are today used in medium and large power applications. There are three major topologies of multilevel inverters; they are capacitor clamped, diode camped and cascaded. In literature it is found that these topologies have been used by several researchers. In this paper single phase cascaded Asymmetrical Multilevel Inverter (AMLI) consisting of two full bridges with unequal DC sources creates a seven level single phase AC output voltage. Due to switch combination redundancies, there are certain degrees of freedom to generate the seven level AC output voltage. Shoji Fukuda and Kunio Suzuki [1] have proposed and used the carrier PWM schemes for the conventional three phase square wave inverter and the three phase three level inverters.
It was later found by researchers that the same can be applied to the multilevel inverter topologies. Tolbert and Habetler [2] have used the multicarrier techniques for the evaluation of the six level diode clamped NPC (Neutral Point Clamped) inverters. Further they have evaluated the performance of the inverter using the THD and the RMS (fundamental) value of output voltage and the maximum utilization of the DC bus voltages. Further Leon Tolbert et al [3] proposed some novel multilevel PWM strategies to take advantage of the multiple levels in both a diode clamped inverter and cascaded H-bridge inverter by utilizing all of the levels in the inverter even at low modulation indices. An analytical approach of the carrier based Pulse Width Modulation (PWM) technique has been discussed by Brendan Peter McGrath and Donald Grahame Holmes[4]. A new clew for research on PWM methods for MLI is found in [5] and [6] deals with sine PWM methods for MLI in the over modulation region. Chunmei Feng and Agelidis [7] have used the NPC topology for evaluation of THD using multicarrier PWM schemes. This carrier technique reduces harmonics because of the Control Freedom Degree (CFD) and this was proposed by Shanthi and Natarajan [8]. Brendan Peter McGrath et al [9] have presented a similar equivalence between the Phase Disposition (PD) carrier and space vector modulation strategies applied to diode clamped, cascaded N-level or hybrid multilevel inverters.
Dae-Wook Kang et al [10] have proposed an improved carrier-based Space Vector PWM is ISPWM scheme, which is fully suitable for cascaded multilevel inverter topologies because it can achieve the optimized switch utilization through the redistribution of the triangular carrier waves considering leg voltage redundancies while having the advantages of the conventional carrier-based SVPWM. Ben-brahim and Tadakuma [11] have proposed that the fluctuations of the neutral-point voltage are also reduced using this switch pattern method. This paper presents a single phase cascaded AMLI topology for investigation with COPWM using various references.
The gating pulses for the inverter is generated for various references (sine, trapezoidal and TAR) and multicarrier overlapping pulse width modulation strategy (Type A, Type B and Type C). The asymmetrical single phase cascaded inverter requires four PWM pulses for the positive switching and four PWM pulses for the negative switching within the time span of 20ms seconds to obtain a frequency of 50 Hz. The carriers are compared with the three reference waves and PWM is generated for each of the bands. PWM arrangement is simulated for the single phase cascaded AMLI (Fig.1) in the MATLAB /SIMULINK environment as in Fig.2.

II.MODULATION STRATERGIES FOR MULTILEVEL INVERTER
The high number of switches composing a multilevel converter may lead to the conclusion that complex algorithms are necessary. The modulation algorithm used to drive the multilevel converter has to be aimed to give the voltage level required for each leg; the translation in the proper switch configuration is done by other algorithms which can be hardware or software implemented. The modulation strategy used here is the multicarrier carrier overlapping pulse width modulation. This paper presents three COPWM methods that utilize the CFD of vertical

offsets among carriers. They are COPWM-A, COPWM- B, COPWM-C. The above three methods are simulated in this paper. For an m-level inverter using carrier overlapping technique, m-1 carriers with the same frequency f_c and same peak-to-peak amplitude A_c are disposed such that the bands they occupy overlap each other: the overlapping vertical distance between each carrier is $A_c/2$. The reference waveform has amplitude of A_m and frequency of f_m and it is centered in the middle of the carrier signals. The reference wave is continuously compared with each of the carrier signals. If the reference wave is more than a carrier signal, then the active devices corresponding to that carrier are switched on. Otherwise, the device switches off. The amplitude modulation index m_a and the frequency ratio m_f are defined in the carrier overlapping method as follows:

$$m_a = A_m/((m/4)* A_c)$$

$$m_f = f_c / f_m$$

In this paper, mf =40, A_c=1.6 and m_a is varied from 0.7 to 1.The vertical offset of carriers for seven-level inverter with COPWM-A strategy method is shown in Fig.3. It can be seen that the three carriers are overlapped in the positive side and three are overlapped in the negative side with other and the reference sine wave is placed at the middle of the six carriers. Similarly in the COPWM-B it can be seen that the carriers are set opposite in the negative side totaling six carriers (Fig.4).

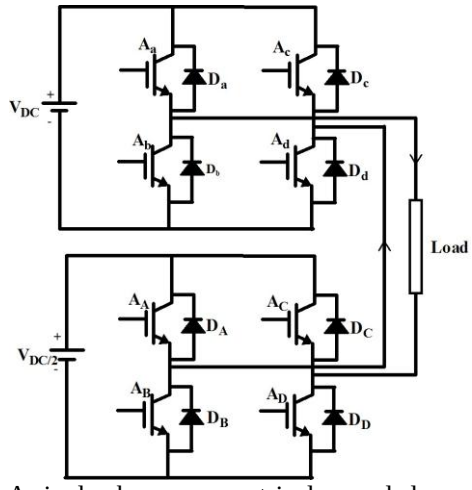

Fig.1. A single phase asymmetrical cascaded seven level inverter

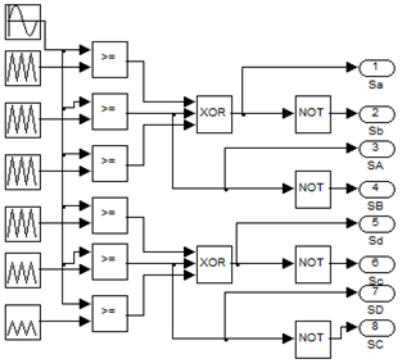

Fig.2.SIMULINK model developed for single phase PWM strategy.

CARRIER OVERLAPPING PWM WITH SINE REFERENCE

Instead of maintaining the width of all pulses the same as in the case of multiple pulse width modulation, the width of each pulse is varied in proposition to the amplitude of a sine wave evaluated at the center of the same pulse. The distortion factor and the lower order harmonics are reduced significantly. This PWM technique is used in industrial applications and is called as sine SPWM. Figs.3-5 show the carrier arrangement with sine reference for COPWM strategy for m_a= 0.8

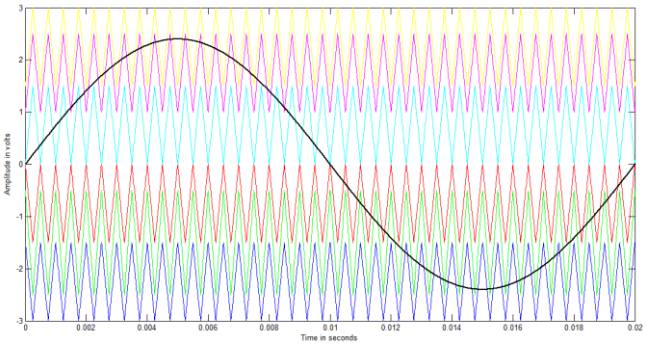

Fig.3. Carrier arrangement for COPWM-A strategy (m_a=0.8) with sine reference

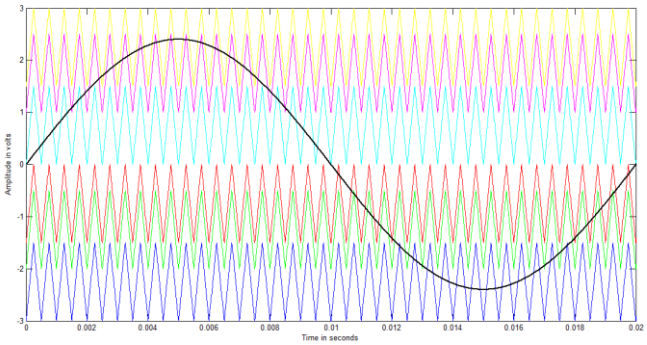

Fig.4. Carrier arrangement for COPWM-B strategy (m_a=0.8) with sine reference

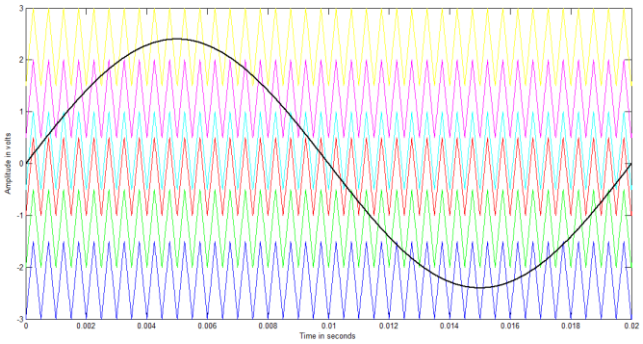

Fig.5. Carrier arrangement for COPWM-C strategy (m_a=0.8) with sine reference

COPWM WITH TRAPEZOIDAL REFERENCE

The trapezoidal wave can be obtained from a triangular wave by limiting its magnitude to $\pm A_r$ which is related to the peak value of $A_{r(max)}$ by $A_r=\sigma A_{r(max)}$ where σ is called the triangular factor because the waveform becomes a triangular wave when σ=1. Here it is taken as σ = 0.5. The modulation index m_a is

$$m_a = A_r/A_c$$

A_r = Amplitude of reference
A_c = Amplitude of carrier

Fig.6-8 show the carrier for modulation strategy with trapezoidal reference.

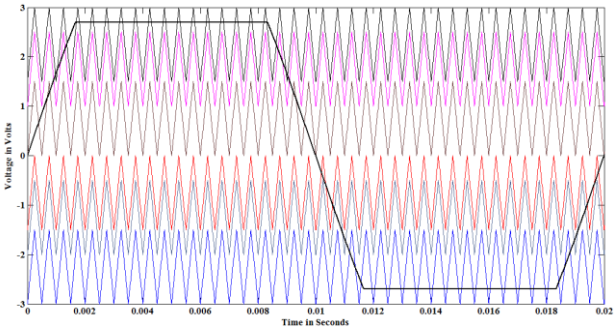

Fig.6. Carrier arrangement for COPWM-A strategy (m_a=0.8) with trapezoidal reference

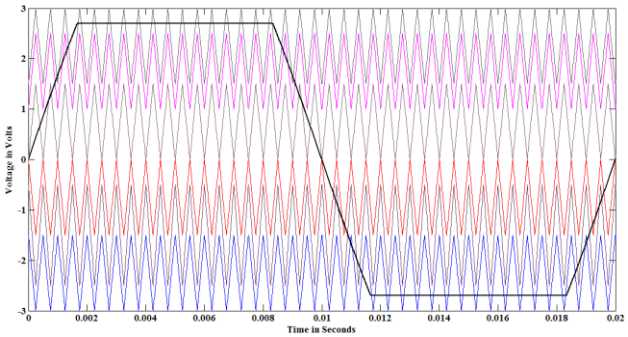

Fig.7. Carrier arrangement for COPWM-B strategy (m_a=0.8) with trapezoidal reference

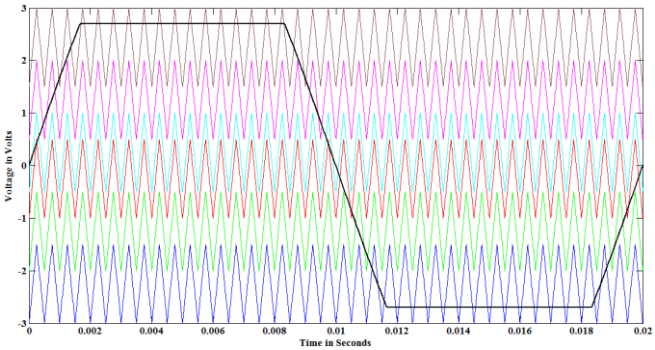

Fig.8. Carrier arrangement for COPWM-C strategy (m_a=0.8) with trapezoidal reference

CARRIER OVERLAPPING PWM WITH TAR REFERENCE

The TAR reference is obtained by amalgamation of The triangular wave and the trapezoidal wave with σ = 0.5 Such TAR is used as reference to generate gating pulses for the chosen asymmetrical seven level inverter with COPWM. Figs.9-11 show carrier for modulation strategy with TAR reference.

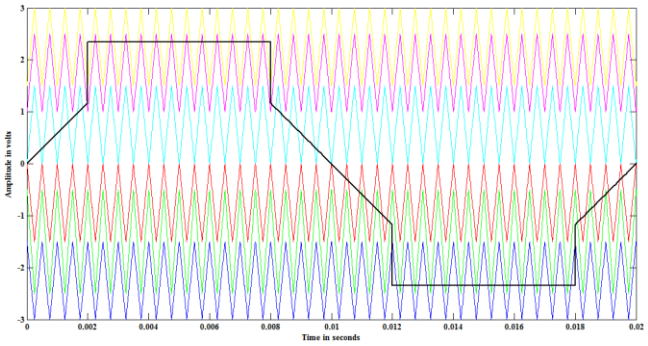

Fig.9 Carrier and TAR reference arrangements for COPWM-A modulation strategy

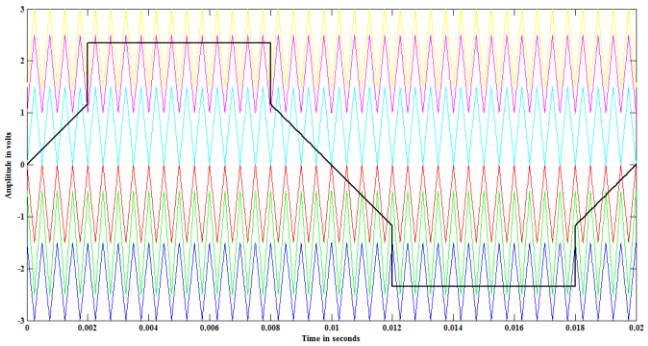

Fig.10 Carrier and TAR reference arrangements for COPWM-B modulation strategy

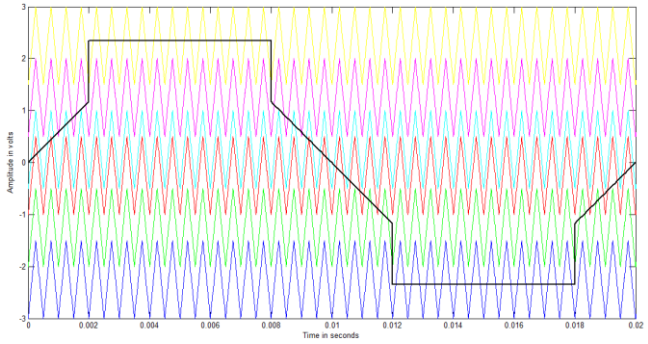

Fig.11. Carrier and TAR reference arrangements for COPWM-C modulation strategy

III. SIMULATION RESULTS

THD can obtained by applying Fourier transforms. These are taken care in the MATALAB /SIMULINK by the Graphical User Interface (GUI) tool used in MATLAB SIMULINK environment. The RMS (fundamental) output voltage is higher in the **COPWM-C** with all references. The THD with the COPWM-C and sine and TAR reference is lower. Fig.12. shows the FFT spectrum for COPWM-A strategy with sine reference. Fig.13.displays the FFT spectrum for COPWM-B strategy with sine reference. Fig.14. portrays the FFT spectrum for COPWM-C strategy with sine reference. Fig.15-17 display the respective FFT spectra for COPWM-A,B,C strategies with trapezoidal reference.

Fig.18-20 shows FFT spectra for COPWM-A,B,C strategy with TAR reference. Fig.21 displays the seven level output voltage generated by COPWM-A switching strategy with sine reference. Fig.22 shows the seven level output voltage generated by COPWM-B switching strategy with trapezoidal reference. Fig.23 shows the seven level output

voltage generated by COPWM-C switching strategy with TAR reference.

Fig.24. shows a graphical comparison of %THD for various strategies for different modulation indices. The following parameter values are used for simulation: V_{DC} =100V, $V_{DC/2}$=50 A_c=1.6, m_f=40 and R (load) = 100 ohms.

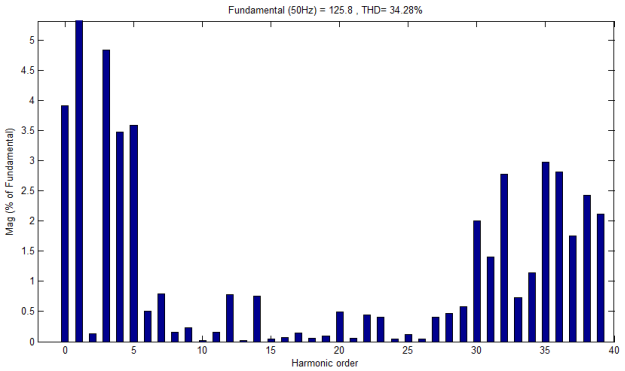

Fig.12. FFT spectrum for COPWM-A strategy with sine reference

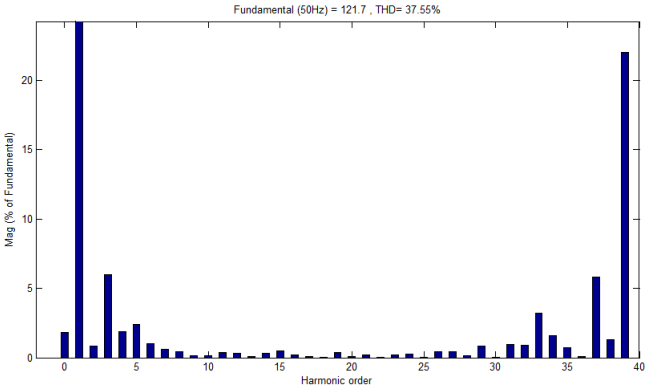

Fig.13. FFT spectrum for COPWM-B strategy with sine reference

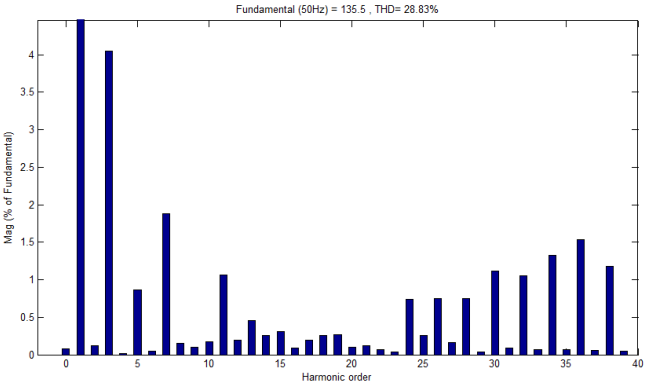

Fig.14. FFT spectrum for COPWM-C strategy with sine reference

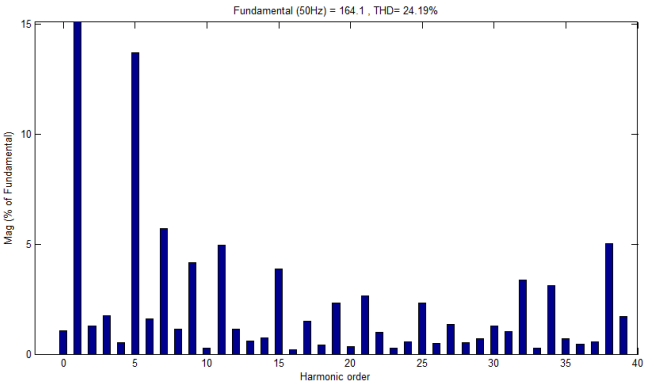

Fig.15. FFT spectrum for COPWM-A strategy with trapezoidal reference

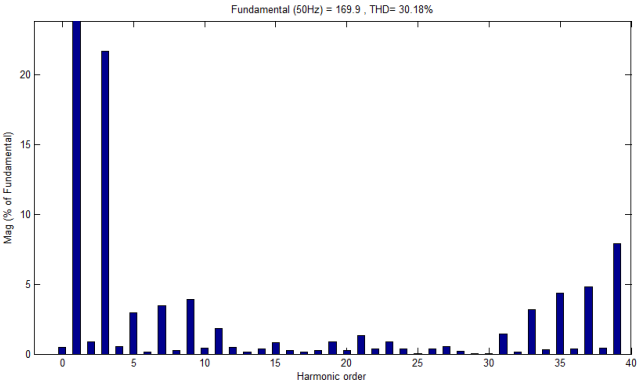

Fig.16. FFT spectrum for COPWM-B strategy with trapezoidal reference

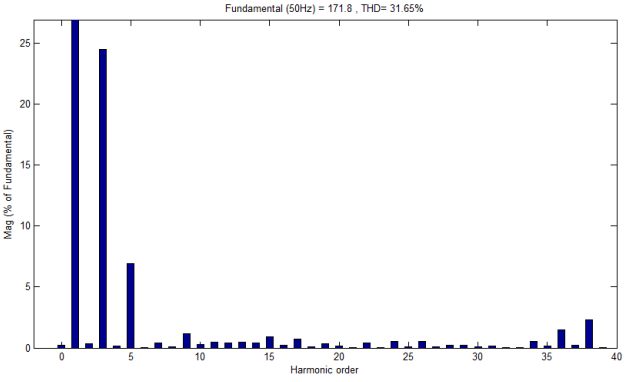

Fig.17. FFT spectrum for COPWM-C strategy with trapezoidal reference

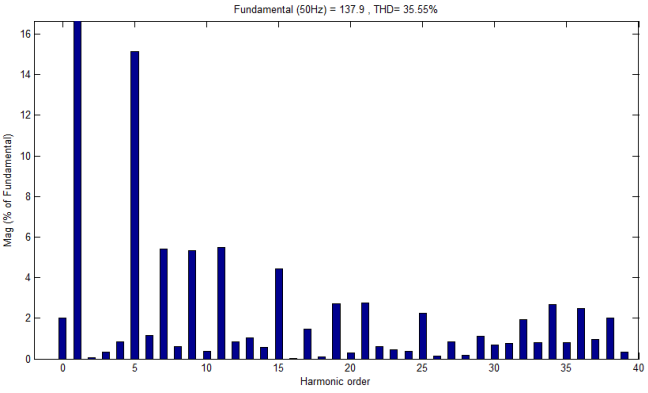

Fig.18. FFT spectrum for COPWM-A strategy for with TAR reference

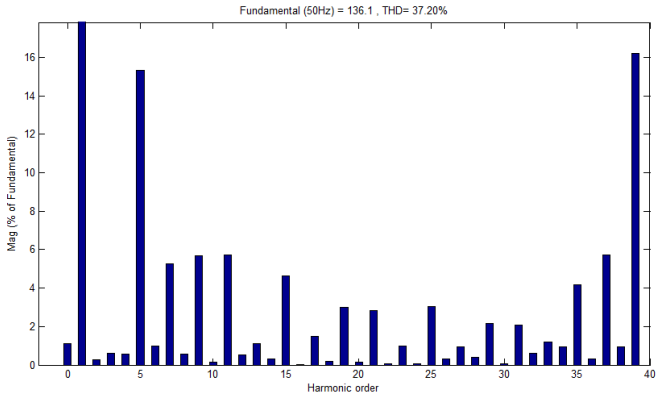

Fig.19. FFT spectrum for COPWM-B strategy for with TAR reference.

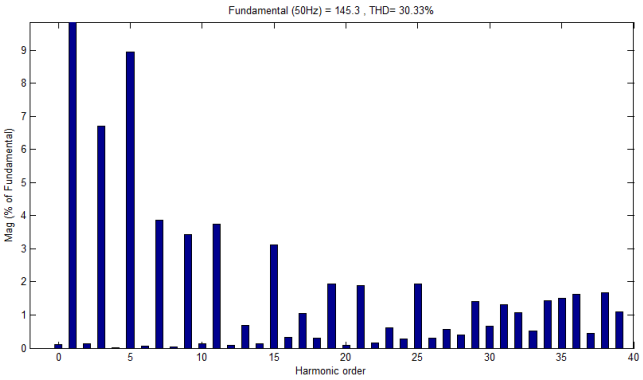

Fig.20. FFT spectrum for COPWM-C strategy for with TAR reference

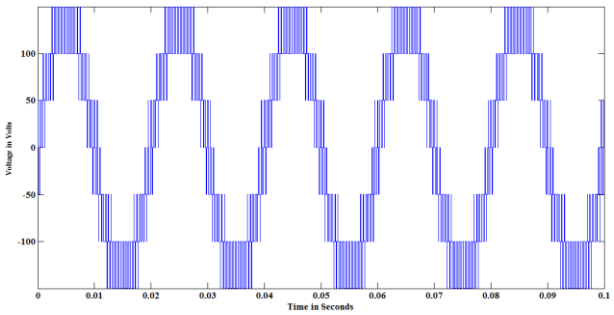

Fig.21.Output voltage generated by COPWM-A. (sine reference)

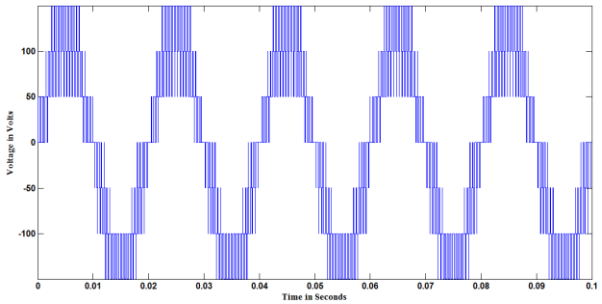

Fig.22.Output voltage generated by COPWM-B. (Trapezoidal reference)

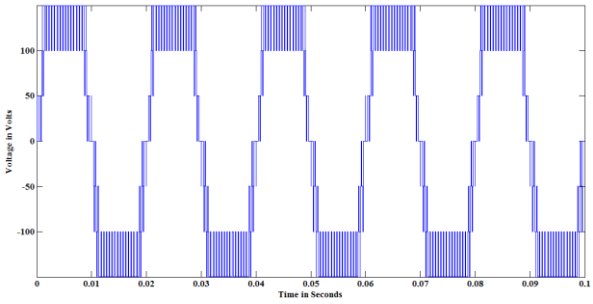

Fig.23. Output voltage generated by COPWM-C. (TAR reference)

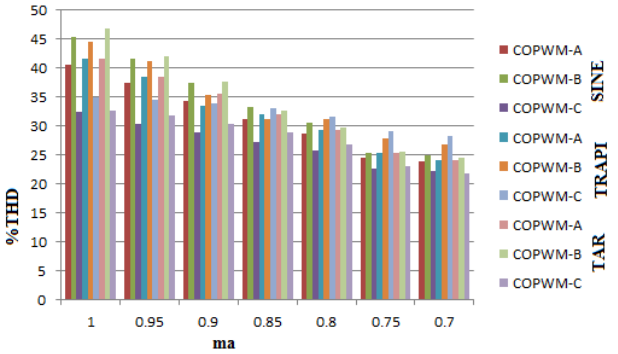

Fig.24.%THD Vs ma

Table-I
%THD of output voltage of AMLI for different COPWM stratergies with sine referrence

m_a	COPWM-A	COPWM-B	COPWM-C
1	23.91	24.89	22.14
0.95	24.47	25.33	22.68
0.9	28.73	30.50	25.84
0.85	31.18	33.32	27.28
0.8	34.28	37.55	28.83
0.75	37.49	41.71	30.33
0.7	40.61	45.42	32.45

Table-II
%THD of output voltage of AMLI for different COPWM strategies with trapezoidal reference

m_a	COPWM-A	COPWM-B	COPWM-C
1	24.19	26.88	28.28
0.95	25.31	27.77	29.11
0.9	29.41	31.18	31.65
0.85	32.08	31.25	32.97
0.8	33.55	30.18	31.65
0.75	38.56	41.16	34.59
0.7	41.64	44.50	34.88

Table-III
%THD values of output voltage of AMLI for different COPWM strategies with TAR reference

m_a	COPWM-A	COPWM-B	COPWM-C
1	41.64	46.91	32.60
0.95	38.56	41.96	31.74
0.9	35.55	37.72	30.33
0.85	32.08	32.72	28.92
0.8	35.55	37.20	30.33
0.75	25.31	25.63	22.96
0.7	24.19	24.46	21.77

Table-IV
RMS (fundamental) of output voltage of AMLI for different COPWM stratergies with sine reference

m_a	COPWM-A	COPWM-B	COPWM-C
1	108.50	107.30	112.20
0.95	107.20	106.00	111.00
0.9	99.50	97.61	104.30
0.85	94.54	92.31	100.20
0.8	88.93	86.08	95.84
0.75	82.85	79.26	91.28
0.7	76.71	72.71	86.26

Table-V
RMS (fundamental) of output voltage of AMLI for different COPWM trapezoidal stategies with sine reference

m_a	COPWM-A	COPWM-B	COPWM-C
1	116.30	129.30	130.30
0.95	114.30	127.50	128.60
0.9	107.50	120.10	121.50
0.85	102.40	115.50	117.10
0.8	91.51	108.60	112.60
0.75	91.30	100.10	108.20
0.7	85.74	92.76	103.60

Table-VI
RMS (fundamental) of output voltageof AMLI for different COPWM with TAR reference

m_a	COPWM-A	COPWM-B	COPWM-C
1	116.00	115.6	119
0.95	114.30	113.9	117.4
0.9	107.50	107.2	110.8
0.85	102.40	101.7	106.1
0.8	97.51	96.23	102.7
0.75	91.30	88.58	97.96
0.7	85.14	81.57	94.56

Table-VII
FF of output voltage of AMLI for different COPWM with sine reference

m_a	COPWM-A	COPWM-B	COPWM-C
1	3.39E+01	6.92E+01	1.50E+03
0.95	3.32E+01	6.84E+01	7.40E+02
0.9	2.60E+01	5.74E+01	1.00E+09
0.85	2.16E+01	4.62E+01	9.93E+08
0.8	1.81E+01	3.83E+01	9.58E+02
0.75	1.42E+01	2.94E+01	4.56E+02
0.7	1.23E+01	2.64E+01	8.63E+02

Table-VIII
FF of output voltage of AMLI for different COPWM with trapezoidal reference

m_a	COPWM-A	COPWM-B	COPWM-C
1	6.65E+01	1.62E+02	4.74E+02
0.95	6.35E+01	1.50E+02	3.03E+02
0.9	6.52E+01	1.41E+02	3.24E+02
0.85	5.85E+01	1.28E+02	5.86E+02
0.8	3.33E+01	1.45E+02	1.13E+03
0.75	2.43E+01	6.46E+01	1.08E+03
0.7	1.56E+01	5.01E+01	2.07E+03

Table-IX
FF of output voltage of AMLI for different COPWM with TAR reference

m_a	COPWM-A	COPWM-B	COPWM-C
1	6.63E+01	1.10E+02	1.19E+03
0.95	6.35E+01	1.04E+02	7.83E+02
0.9	6.52E+01	1.02E+02	7.39E+02
0.85	5.85E+01	1.07E+02	2.12E+03
0.8	3.55E+01	6.42E+01	6.85E+02
0.75	2.43E+01	6.56E+01	4.90E+02
0.7	1.55E+01	4.29E+01	1.89E+03

TABLE-X
3rd and 5th harmonics for various references with different COPWM strategies

TYPE OF CARRIER	3rd Harmonic	5th Harmonic
COPWM-A-SINE	4.83	3.59
COPWM-B-SINE	5.99	2.38
COPWM-C-SINE	4.05	**0.87**
COPWM-A-TRAPI	22.26	3.74
COPWM-B-TRAPI	21.67	2.94
COPWM-C-TRAPI	24.46	6.09
COPWM-A-TAR	18.3	4.81
COPWM-B-TAR	11.7	7.24
COPWM-C-TAR	20.74	7.03

IV.CONCLUSION

Single phase seven level cascaded asymmetrical multilevel inverter employing different multi carrier offset modulation schemes have been investigated. It is found that the DC bus utilization is high in COPWM-C modulation strategy with all references as shown in Table III-V. The THD is less in COPWM-C with sine and TAR references.

REFERENCES

[1] Shoji Fukuda, Konia Suzuki"Using Harmonic Distortion Determining Factor for Harmonic Evaluation of Carrier-Based PWM Methods", *IEEE Industry Applications Society, October 5-9, 1997.*

[2] M.Leon Tolbert, G.Thomas. Habetler, "Novel Multilevel Inverter Carrier-Based PWM Method", *IEEE Transactions on Industry Applications, Vol. 35, No. 5, September/October 1999.*

[3] Leon M. Tolbert, Fang Zheng Peng, , and Thomas G. Habetler, "Multilevel PWM Methods at Low Modulation Indices"*IEEE Transactions on Power Electronics, Vol. 15, No. 4, July 2000 719*

[4] Brendan Peter McGrath, Donald Grahame Holmes, "An Analytical Technique for the Determination of Spectral Components of Multilevel Carrier-Based PWM Methods", *IEEE Transactions on Industrial Electronics, Vol. 49, No. 4, August 2002.*

[5] Hongyang WU, Yan DENG, Ying LIU, Xiangning HE, "A New Clew for Research on PWM Methods of Multilevel Inverters: Principle And Applications", *PCC-Osaka 2002.*

[6] Brendan Peter McGrath and Donald Grahame Holmes, "Sinusoidal PWM of Multilevel Inverters in the Over modulation Region", *IEEE 2002.*

[7] Chunmei Feng and G.Vassilios Agelidis, "On the Comparison of Fundamental and High Frequency Carrier-Based PWM Techniques for Multilevel NPC Inverters", *IEEE Conference 2002.*

[8] B.Shanthi and S.P.Natarajan 'Comparative study on various unipolar PWM strategies for single phase five level cascaded inverter', *International Journal of Power Electronics (IJPELEC), Special issue on: Power Converters: Modeling, Simulation, Analysis, Topologies, Secondary issues and Applications, InderScience Publication, Switzerland, pp.36-50, 2009.*

[9] Brendan Peter McGrath, Donald Grahame Holmes and Thomas Lipo,"Optimized Space Vector Switching Sequences for Multilevel Inverters *IEEE Transactions on Power Electronics, Vol. 18, No. 6, November 2003.*

[10] Dae-Wook Kang, Yo-Han Lee, Bum-Seok Suh, Chang-Ho Choi and Dong-Seok Hyun, An Improved Carrier-Based SVPWM Method Using Leg Voltage Redundancies in Generalized Cascaded Multilevel Inverter Topology. *IEEE Transactions on Power Electronics, Vol. 18, No. 1, January 2003*

[11] L.Ben-brahim and S.Tadakuma, Novel Multilevel Carrier Based PWM Control Method for GTO Inverter in Low Index Modulation Region *IEEE Transactions on Power Electronics, Vol. 18, No. 1, January 2006 42*(1), 121-127.